Full RF Characterization for Extracting the Small-Signal Equivalent Circuit in Microwave FET's

J. Apolinar Reynoso-Hernández, Francisco Elías Rangel-Patiño, and Julio Perdomo

Abstract—**The basic cell for linear, nonlinear, and noise models is the intrinsic transistor. To determine the intrinsic device elements a de-embedding of the parasitic elements is needed. A good extraction of the extrinsic device elements along with a suitable topology leads to the true values of the intrinsic transistor and therefore to good models. In this paper, three methods for access resistances computation are investigated. Two of them are based on DC measurements with floating drain or source and they use a modified Schottky model for determining the gate resistance. The third method is an improved cold-FET technique based on RF measurements with floating drain instead of the $V_{DS} = 0$ condition. The originality of the proposed RF method is the use of the floating drain configuration which overcomes the inconsistencies between DC and RF methods. On the other hand, extended expressions for parasitic inductances calculation are presented. These expressions take into account the influence of different factors such as parasitic capacitances and access resistances. Based on both, the improved cold-FET technique for access resistances computation, and the extended equations for parasitic inductances, this paper presents also an alternative method for extracting the small-signal equivalent circuit on PHEMT's by means of RF measurements only, with no optimization procedures.**

I. Introduction

THE small-signal equivalent circuit of microwave GaAs FET's is crucial for noise modeling, suitable for microwave CAD and very useful for device characterization. To extract the value of the equivalent circuit model elements two approaches are often used. The first approach uses both RF measurements and optimization methods [1], while the second one uses DC and RF measurements only [2] and [3]. Both approaches lead to good results: measured and calculated S parameters agree well with each other. However, the first approach depends strongly on both the initial values for starting the optimization procedure and the optimization procedure itself. In addition, this approach may yield element values with no physical sense, e.g., a negative value for a resistance, and therefore, it may not be suitable for device performance evaluation [4]. To overcome this problem the second approach seems to be more reliable.

A number of small-signal equivalent circuit topologies exist for microwave FET's modeling. The main differences among them rest in the parasitic elements location, which depends on the transistor geometry and on the transistor embedding medium. For example, the equivalent circuit shown in Fig. 1(a) is recommended for transistors embedded in chip carriers [2], while the equivalent circuits depicted in Fig. 1(b) and (c) are advised for coplanar transistors [5] and [6].

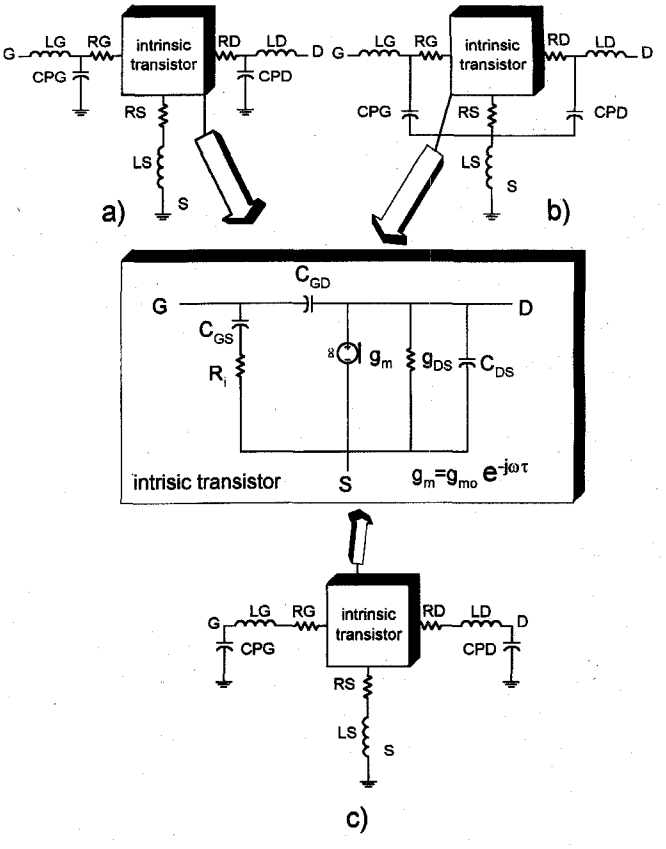

Fig. 1. Circuit topologies previously reported in the literature [2], [5], and [6].

Independently of topology, equivalent circuit elements can be grouped in two categories: extrinsic or parasitic elements, which are bias independent (R_S, R_D, R_G, L_S, L_D, L_G, C_{PG}, and C_{PD}), and intrinsic elements, which are bias dependent (C_{GS}, C_{GD}, C_{DS}, R_i, g_{DS}, g_m, and τ). Extrinsic elements and especially access resistances (R_S, R_D, and R_G), are very difficult to compute from electrical measurements. Previous techniques, based on DC or RF measurements [7]–[13], have been put forward to estimate these resistances. The main problem up to now lies in the fact that the results of both techniques are not consistent with each other.

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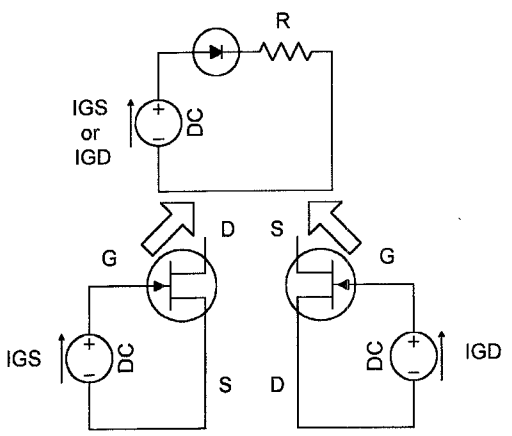

Fig. 2. Schottky diode model for transistors with floating drain or source.

On the other hand, it has been our experience that Z parameter equations [2] currently used for determining parasitic inductances may yield negative values with no physical sense. This behavior has been observed in the case of source inductance L_S for on-wafer coplanar transistors.

The purpose of this paper is firstly, to set DC and RF techniques for access resistances estimation such as to they agree with each other. Secondly, the present work aims to extend Dambrine's Z parameter equations in order to they apply to all kinds of transistors.

DC and RF methods for computing access resistances are described in Sections II and III, respectively. Section IV deals with the parasitic inductances determination from extended Dambrine's equations. Finally, experimental results are presented in Section V, where a full RF extraction of the small-signal equivalent circuit is carried out for a on-wafer coplanar PHEMT using no optimization methods and in the frequency range 0.045–20 GHz.

II. DC Method for Access Resistances Evaluation

From a experimental point of view, the method proposed for access resistances evaluation consists in the measurement of $I_G(V_D)$ and $I_G(V_G)$ characteristics at forward bias ($V_G > V_{bi} > 0$) with floating drain or source (I_G equals I_{GS} or I_{GD}, V_D equals V_{DS} or V_{SD} and V_G equals V_{GS} or V_{GD} with floating drain or source, respectively). The measurements principle is illustrated in Fig. 2. From a theoretical point of view, the R^{end} technique is used along with a modified Schottky diode model. Theory leads to the resolution of a simultaneous linear equations system where R_S, R_D, and R_G are the unknowns.

A. The R^{end} Technique

From the circuit shown in Fig. 2, the V_D voltage due to I_G current can be written as

$$V_D = I_G R^{end} \tag{1}$$

where R^{end} is the circuit resistance ($R^{end} = R_S^{end}$ or R_D^{end} with floating drain or source, respectively).

A priori, R^{end} could be expected to have a single component R_* ($R_* = R_S$ or R_D with floating drain or source, respectively). However, due to gate current distribution, a fraction of V_D voltage drops in the channel resistance R_{CH}. Based on this assumption K. M. Lee *et al.* [8] suggest that an supplementary resistance $\alpha_t R_{CH}$ have to be added to R_*. Concerning α_t value, it has been reported [8], [9] that $\alpha_t = 1/2$. Under these conditions R^{end} is given by

$$\begin{aligned} R^{end} &= R_S^{end} \\ &= R_S + \frac{R_{CH}}{2} \qquad \text{with floating drain} \end{aligned} \tag{2}$$

$$\begin{aligned} R^{end} &= R_D^{end} \\ &= R_D + \frac{R_{CH}}{2} \qquad \text{with floating source} \end{aligned} \tag{3}$$

where R_S, R_D, and R_{CH} are the unknowns. These expressions constitute the first two equations of the system to be solved.

On the other hand, from $I_G(V_D)$ measurements and according to (1), R^{end} values are computed as the slope of V_D versus I_G

$$R_S^{end} = \left(\frac{V_{DS}}{I_{GS}}\right)_{\text{floating drain}} \tag{4}$$

$$R_D^{end} = \left(\frac{V_{SD}}{I_{GD}}\right)_{\text{floating source}} \tag{5}$$

B. The Planar Schottky Diode Model

Up to here, equations involving R_S and R_D have been established [(2) and (3)]. However, for a full computation of access resistances, equations involving the gate resistance R_G are needed. The originality of the proposed DC method rests in the use of a modified Schottky diode model for taking into account R_G.

Under floating drain or source conditions, the transistor is formed, respectively, by gate-source or gate-drain contacts only. Then, the transistor is modeled by a real planar Schottky diode illustrated in Fig. 2. Under forward bias condition ($V_G > V_{bi} > 0$), the current I_G flowing through the diode is given by

$$I_G = I_S \cdot \exp\left(\frac{V}{nU_T}\right) \tag{6}$$

where

- I_S saturation current (A): $I_S = (I_S)_S$ or $(I_S)_D$ with floating drain or source;
- V voltage across the ideal Schottky diode (V);
- n ideality factor of the real Schottky diode: $n = n_S$ or n_D with floating drain or source;
- U_T thermal potential (V): $U_T = kT/q$;
- k Boltzmann constant (J/K);
- T absolute temperature (K);
- q electron charge (C).

The saturation current is given by

$$I_S = S \cdot A^{**} \cdot T^2 \cdot \exp\left(\frac{-V_{bi}}{U_T}\right) \tag{7}$$

where

- S gate surface (cm^2);
- A^{**} Richardson constant (A $\text{cm}^{-2}\text{K}^{-2}$);
- V_{bi} Schottky barrier height (V).

The voltage V across the ideal diode can be expressed in terms of the external positive voltage V_G and the voltage drop across the series resistance R associated with the real Schottky diode

$$V = V_G - I_G R. \tag{8}$$

Substituting (8) into (6) and assuming that $V_G > 3kT/q$, (6) becomes

$$I_G = I_S \cdot \exp\left(\frac{V_G - I_G R}{nU_T}\right) \tag{9}$$

then

$$V_G = RI_G + nU_T \ln(I_G) - nU_T \ln(I_S). \tag{10}$$

Let define $R^{(S)}$ and $R^{(D)}$ as the values of the series resistance R, with floating drain or source respectively. In the case of the transistor, it has been shown that R can be written as [9]

$$R^{(S)} = R_S + R_G + \alpha_i R_{CH} \tag{11}$$
$$R^{(D)} = R_D + R_G + \alpha_i R_{CH} \tag{12}$$

where α_i is a factor equal to 1/3 and R_S, R_D, R_G, and R_{CH} are the unknowns. These expressions complete the system to be solved.

As for $R^{(S)}$ and $R^{(D)}$ coefficients, their values are calculated according to either of the two following methods, based on $I_G(V_G)$ measurements.

C. First Method for the Computation of the Schottky Diode Series Resistance

This method, inspired from the work reported in [14], consists in the least squares optimization of the analytical function that predicts the $I(V)$ characteristics of a real Schottky diode (10). This function is of the form

$$V_G = RI_G + a \ln(I_G) + b \tag{13}$$

where coefficients R, a and b are the variables to be optimized. The expressions of a and b are given by

$$a = nU_T \tag{14}$$
$$b = -a \ln(I_S). \tag{15}$$

With the help of m measurements of current I_G for m values of voltage V_G it is possible to define the error function X to be minimized

$$X = \sum_{i=1}^{m} [RI_{Gi} + a \ln(I_{Gi}) + b - V_{Gi}]^2. \tag{16}$$

The minimum of X occurs when the partial derivatives with respect to R, a, and b are equal to zero. These conditions lead to a set of three simultaneous linear equations where R, a, and b are the unknowns. The resulting equations can be written under matrix form as

$$\mathbf{E} \cdot \mathbf{Y} = \mathbf{F} \tag{17}$$

where

$$\mathbf{E} = \begin{bmatrix} \sum_{i=1}^{m} (I_{Gi})^2 & \sum_{i=1}^{m} (I_{Gi})(\ln I_{Gi}) & \sum_{i=1}^{m} (I_{Gi}) \\ \sum_{i=1}^{m} (I_{Gi})(\ln I_{Gi}) & \sum_{i=1}^{m} (\ln I_{Gi})^2 & \sum_{i=1}^{m} (\ln I_{Gi}) \\ \sum_{i=1}^{m} (I_{Gi}) & \sum_{i=1}^{m} (\ln I_{Gi}) & m \end{bmatrix} \tag{18}$$

$$\mathbf{Y}^T = (R \quad a \quad b) \tag{19}$$

$$\mathbf{F}^T = \begin{bmatrix} \sum_{i=1}^{m} (I_{Gi})(V_{Gi}) & \sum_{i=1}^{m} (\ln I_{Gi})(V_{Gi}) & \sum_{i=1}^{m} (V_{Gi}) \end{bmatrix}. \tag{20}$$

After resolution of (17), all Schottky diode physical parameters can be obtained: the series resistances R, the ideality factor n ($n = a/U_T$) and the saturation current I_S [$I_S = \exp(-b/a)$].

D. Second Method for the Computation of the Schottky Diode Series Resistance

This method, developed after the procedure reported in [15], deals with the optimization of the linear relationship between the variables $(\partial V_G/\partial \ln I_G)$ and I_G in the positive region of the Schottky diode $I(V)$ characteristic. Calculating the partial derivative of V_G (13) with respect to $\ln(I_G)$ we have

$$\frac{\partial V_G}{\partial \ln I_G} = RI_G + a. \tag{21}$$

Equation (21) characterizes a straight line with R as slope and a as y-axis intercept. Carrying out a set of m measurements of current I_G for m values of voltage V_G it is possible to compute $(m-1)$ mean values of the derivative $(\partial V_G/\partial \ln I_G)$

$$\left\{\frac{\Delta V_{G1}}{\Delta \ln I_{G1}}, \frac{\Delta V_{G2}}{\Delta \ln I_{G2}}, \cdots, \frac{\Delta V_{Gi}}{\Delta \ln I_{Gi}}, \cdots, \frac{\Delta V_{G(m-1)}}{\Delta \ln I_{G(m-1)}}\right\}$$

where

$$\frac{\Delta V_{Gi}}{\Delta \ln I_{Gi}} = \frac{V_{G(i+1)} - V_{Gi}}{\ln I_{G(i+1)} - \ln I_{Gi}} \tag{22}$$

Using the $(m-1)$ computed $(\Delta V_G/\Delta \ln I_G)$ values and the corresponding $(m-1)$ measured I_G values, R and a, the coefficients of (21), are calculated by means of a least squares optimization procedure. It is noticed that, unlike the first method, the second method does not allow a full extraction of the Schottky diode physical parameters.

E. Extraction of Access Resistances

For the estimation of access resistances, (4), (5), (11), and (12) have to be solved simultaneously. We have a set of four linear equations with four unknowns (R_S, R_D, R_G, and R_{CH}). If R_S and R_D values are derived from (4) and (5), and then are substituted into (11) and (12) the system to be solved becomes

$$R_S + \frac{R_{CH}}{2} = R_S^{end} \tag{23}$$

$$R_D + \frac{R_{CH}}{2} = R_D^{end} \tag{24}$$

$$R_G - \frac{R_{CH}}{6} = R^{(S)} - R_S^{end} \tag{25}$$

$$R_G - \frac{R_{CH}}{6} = R^{(D)} - R_D^{end}. \tag{26}$$

Two equivalent expressions are obtained for the term $(R_G - R_{CH}/6)$ [(25) and (26)]. Hence, if floating drain and floating source DC measurements are consistent with each other, one should find that

$$R^{(S)} - R_S^{end} = R^{(D)} - R_D^{end}. \tag{27}$$

On the other hand, the value of R_{CH} is expected to be very small with respect to those of access resistances. Therefore, R_S, R_D, and R_G are given by

$$R_S = R_S^{end} \tag{28}$$

$$R_D = R_D^{end} \tag{29}$$

$$R_G = [R^{(S)} - R_S^{end}] = [R^{(D)} - R_D^{end}]. \tag{30}$$

III. RF Method for Access Resistances Evaluation

A. DC and RF Inconsistencies

The cold-FET technique for access resistances estimation was proposed by [10]. This technique is based on RF measurements with both large forward bias current in the gate and drain-source voltage equal to zero. Due to V_{DS} = 0 V condition, the gate current is split; it flows not only through the source, but also through the drain. Under this configuration, the series resistance R associated with the Schottky diode is given by

$$R = R_G + \frac{1}{\left[\frac{1}{(R_S + \alpha_1 R_{CH})} + \frac{1}{(R_D + \alpha_2 R_{CH})}\right]} \tag{31}$$

where

- R_{CH} channel resistance;
- α_1 a factor (unknown) related to the gate-source current distribution;
- α_2 a factor (unknown) in connection with the gate-drain current distribution.

This expression is different from that used to model the series resistance when drain is open (11). In order to overcome this inconsistency, the RF cold-FET technique has been modified by changing the bias condition V_{DS} = 0 into floating drain configuration.

B. Z Parameters and Access Resistances Evaluation

The method proposed for access resistances extraction (and for parasitic inductances, *cf.*, Section IV) is based on Z parameters computed from the measurement versus frequency of S parameters at $V_{GS} > V_{bi} > 0$ and at open drain for different I_{GS} currents. At $V_{GS} > V_{bi} > 0$ the PHEMT equivalent circuit depicted in Fig. 1(a) is reduced to the circuit shown in Fig. 3. The corresponding Z parameter expressions

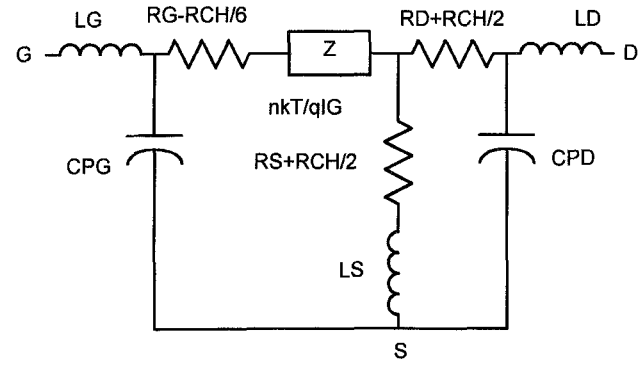

Fig. 3. Small-signal equivalent circuit with floating drain at $V_{GS} > V_{bi} > 0$ for circuit topology reported in Fig. 1(a).

are given as follows. These equations are an extension to those reported by Dambrine *et al.* [2] and are valid for floating drain configuration.

$$Z_{11}(\omega) = \{(R_1 + R_3) + \omega^2 C_{PG}(R_1 + R_3)(L_S - C_{PD}R_3^2)\} + j\omega\{(L_S + L_G) - [C_{PD}R_3^2 + C_{PG}(R_1 + R_3)^2]\} \tag{32}$$

$$Z_{12}(\omega) = \{R_3 + \omega^2 L_S[C_{PD}(R_2 + R_3) + C_{PG}(R_1 + R_3)]\} + j\omega\{L_S - R_3[C_{PD}(R_2 + R_3) + C_{PG}(R_1 + R_3)]\} \tag{33}$$

$$Z_{22}(\omega) = \{(R_2 + R_3) + \omega^2 C_{PD}(R_2 + R_3)(L_S - C_{PG}R_3^2)\} + j\omega\{(L_S + L_D) - [C_{PG}R_3^2 + C_{PD}(R_2 + R_3)^2]\} \tag{34}$$

where

$$R_1 = R_G - \frac{R_{CH}}{6} + \frac{n_S kT}{qI_{GS}} \tag{35}$$

$$R_2 = R_D + \frac{R_{CH}}{2} \tag{36}$$

$$R_3 = R_S + \frac{R_{CH}}{2}. \tag{37}$$

Concerning real parts of Z parameters, at low frequencies ($f < 5$ GHz), terms in ω^2 are small and can be ignored. Hence, at low frequencies, $\mathrm{Re}\,(Z_{ij})$ depend, among parasitic elements, on access resistances only. Their expressions turn equal to those put forward by [2] and apply to open drain condition

$$\mathrm{Re}\,(Z_{11})(\omega) = R_S + R_G + \frac{R_{CH}}{3} + Z_D \tag{38}$$

$$\mathrm{Re}\,(Z_{12})(\omega) = R_S + \frac{R_{CH}}{2} \tag{39}$$

$$\mathrm{Re}\,(Z_{22})(\omega) = R_S + R_D + R_{CH} \tag{40}$$

where

$$Z_D = \frac{n_S kT}{qI_{GS}}. \tag{41}$$

At low frequencies, $\mathrm{Re}\,(Z_{ij})$ are expected to have a constant value, which, except for Z_{11} parameter, is directly related to R_S, R_D, and R_{CH}. Regarding $\mathrm{Re}\,(Z_{11})$, the extraction of access resistances terms is achieved considering that the plot

of $\mathrm{Re}\,(Z_{11})$ versus $1/I_{GS}$ is a straight line with a slope a equal to $a = n_S kT/q$ and with a y-axis intercept $\mathrm{Re}\,(Z_{11})^*$ equal to

$$\mathrm{Re}\,(Z_{11})^* = R_S + R_G + \frac{R_{CH}}{3}. \tag{42}$$

From this plot, the ideality factor n_S is also calculated ($n_S = aq/kT$).

For the computation of R_S, R_D, R_G, and R_{CH}, the system formed by (39), (40), and (42) has to be solved. Substituting R_S value from (39) into (40) and (42), the system becomes

$$R_S + \frac{R_{CH}}{2} = \mathrm{Re}\,(Z_{12}) \tag{43}$$

$$R_D + \frac{R_{CH}}{2} = \mathrm{Re}\,(Z_{22}) - \mathrm{Re}\,(Z_{12}) \tag{44}$$

$$R_G - \frac{R_{CH}}{6} = \mathrm{Re}\,(Z_{11})^* - \mathrm{Re}\,(Z_{12}). \tag{45}$$

These expressions are equivalent to those obtained in the DC method (23)–(26). Finally, if R_{CH} is neglected, access resistances are given by

$$R_S = \mathrm{Re}\,(Z_{12}) \tag{46}$$

$$R_D = \mathrm{Re}\,(Z_{22}) - \mathrm{Re}\,(Z_{12}) \tag{47}$$

$$R_G = \mathrm{Re}\,(Z_{11})^* - \mathrm{Re}\,(Z_{12}). \tag{48}$$

IV. RF Method for Parasitic Inductances Evaluation

This method concerns the imaginary parts of Z parameters calculated from S parameter measurements at $V_{GS} > V_{bi} > 0$ and at open drain bias condition. Z parameter expressions have been given in the previous section.

A. Simplification of $\mathrm{Im}\,(Z_{ij})$ Expressions

Concerning imaginary parts of Z parameters (32)–(34), for microstrip-mounted transistors, due to wire bonding, inductance values are large and the influence of capacitance and access resistances terms can be ignored. Hence, for these transistors, $\mathrm{Im}\,(Z_{ij})$ are related to inductance terms only. Whole equations are reduced into the currently known Dambrine's equations, but they are valid for floating drain configuration

$$\mathrm{Im}\,(Z_{11})(\omega) = \omega(L_S + L_G) \tag{49}$$

$$\mathrm{Im}\,(Z_{12})(\omega) = \omega(L_S) \tag{50}$$

$$\mathrm{Im}\,(Z_{22})(\omega) = \omega(L_S + L_D). \tag{51}$$

It is worth noting that, owing to the form of whole equations (32)–(34), simplified $\mathrm{Im}\,(Z_{ij})$ expressions (49)–(51) hold for all frequencies.

Regarding on-wafer coplanar transistors, inductance values are not large enough anymore to access resistances or capacitance terms be neglected. Then, whole $\mathrm{Im}\,(Z_{ij})$ equations must be used instead of simplified ones.

B. Parasitic Inductances Calculation

In the general case, after transformation of (32)–(34), inductance values are derived as

$$L_G = \frac{\mathrm{Im}\,(Z_{11}) - \mathrm{Im}\,(Z_{12})}{\omega} + (A_{11} - A_{12}) \tag{52}$$

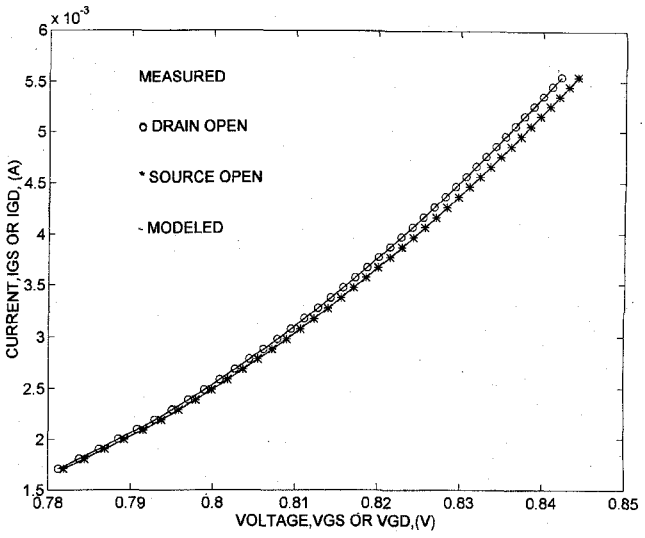

Fig. 4. Gate current I_{GS} or I_{GD} versus gate voltage V_{GS} or V_{GD} for microstrip-mounted transistor with floating drain or source at $V_{GS} > V_{bi} > 0$.

$$L_S = \frac{\mathrm{Im}\,(Z_{12})}{\omega} + A_{12} \tag{53}$$

$$L_D = \frac{\mathrm{Im}\,(Z_{22}) - \mathrm{Im}\,(Z_{12})}{\omega} + (A_{22} - A_{12}) \tag{54}$$

where A_{11}, A_{12}, and A_{22} are factors involving both access resistance and capacitance terms. Their expressions are given by

$$A_{11} = C_{PD}R_3^2 + C_{PG}(R_1 + R_3)^2 \tag{55}$$

$$A_{12} = R_3[C_{PD}(R_2 + R_3) + C_{PG}(R_1 + R_3)] \tag{56}$$

$$A_{22} = C_{PG}R_3^2 + C_{PD}(R_2 + R_3)^2. \tag{57}$$

It should be noticed that if simplified equations are used, $A_{11} = A_{12} = A_{22} = 0$.

V. Results

In order to validate our theoretical investigations, measurements were carried out on two kinds of transistors. A microstrip-mounted PHEMT was used to compare DC and RF methods for access resistances computation. In addition, a on-wafer coplanar PHEMT was used to evaluate the performance of both the RF access resistance method and the extended inductance equations in the extraction of the small-signal equivalent circuit.

A. DC Method for Access Resistances Computation

DC measurements were performed at room temperature on a ultra low noise PHEMT (NE24200 with $W_g = 200\,\mu$m and $L_g = 0.25\,\mu$m) mounted on chip carrier (Intercontinental Microwave®, model A0 102 805), using a computer controlled measurement system formed with Tektronix® equipment (models PS5004, PS5010, and DM5120).

Fig. 4 shows the measured $I_G(V_G)$ characteristics with floating drain or source while Fig. 5 reports the measured $I_G(V_D)$ characteristics with floating drain or source. The plot of the numerical derivative $[dI_G/d\ln(V_G)]$ versus I_G with floating drain or source is shown in Fig. 6.

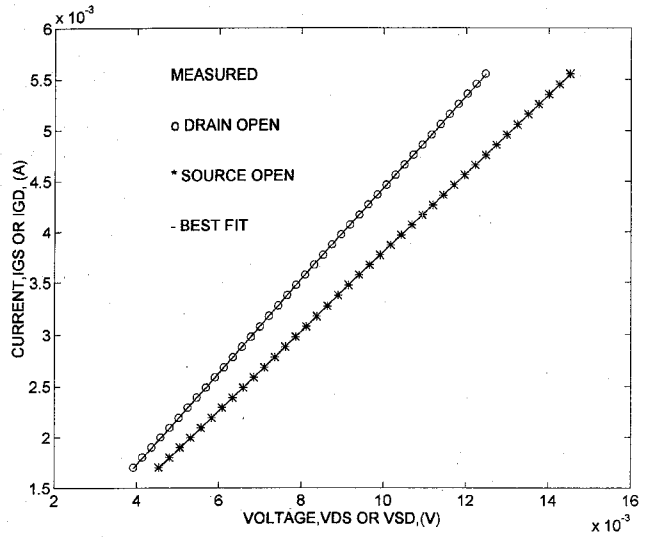

Fig. 5. Gate current I_{GS} or I_{GD} versus drain voltage V_{DS} or V_{SD} for microstrip-mounted transistor with floating drain or source at $V_{GS} > V_{bi} > 0$.

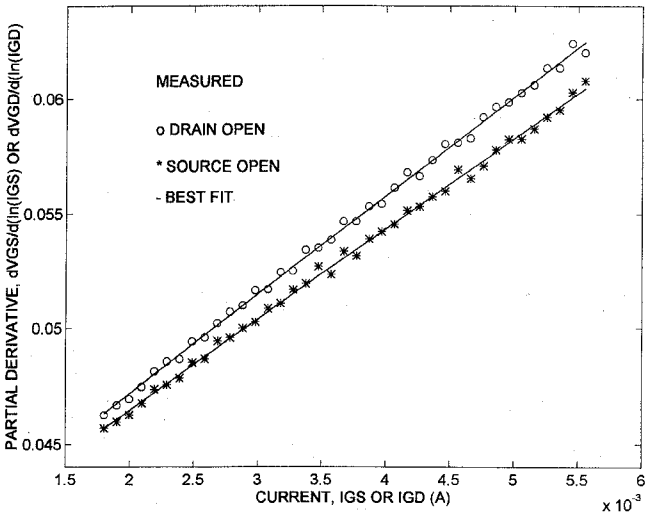

Fig. 6. Partial derivative $\partial(V_{GS})/\partial \ln(I_{GS})$ or $\partial(V_{GD})/\partial \ln(I_{GD})$ versus gate current I_{GS} or I_{GD} for microstrip-mounted transistor with floating drain or source at $V_{GS} > V_{bi} > 0$.

Access resistances were extracted according to theory by means of the measured $I(V)$ characteristics with floating drain or source. Their values are gathered in Table I, along with those of R^{end} resistances and some Schottky diode physical parameters such as the series resistance $R[R = R^{(S)}$ or $R^{(D)}]$, the ideality factor n ($n = n_S$ or n_D) and the saturation gate current I_S [$I_S = (I_S)_S$ or $(I_S)_D$]. It is noticed that the values of series resistances $R^{(S)}$ and $R^{(D)}$, gate resistance R_G and Schottky ideality factors n_S and n_D, computed from the first and second methods agree within <1%. In addition, open drain and open source DC measurements are consistent with each other since the values of $[R^{(S)} - R_S^{end}]$ and $[R^{(D)} - R_D^{end}]$ are equal within 2% (27).

B. RF Method for Access Resistances Computation

S parameter measurements were performed with a network analyzer HP® 8510C and a test fixture Intercontinental

TABLE I
COMPARISON OF DC AND RF METHODS FOR ACCESS RESISTANCES ESTIMATION (VALUES FROM FLOATING DRAIN MEASUREMENTS: $R_G = [R^{(S)} - R_S^{end}]$)

		DC methods		RF method
		1st method	2nd method	
R_S^{end}	(Ω)	2.17		
R_D^{end}	(Ω)	2.37		
$R^{(S)}$	(Ω)	3.87	3.86	
$R^{(D)}$	(Ω)	4.10	4.09	
$\left(R^{(S)} - R_S^{end}\right)$	(Ω)	1.70	1.69	
$\left(R^{(D)} - R_D^{end}\right)$	(Ω)	1.73	1.72	
$\mathrm{Re}(Z_{11})$*	(Ω)			3.73
$\mathrm{Re}(Z_{12})$	(Ω)			2.08
$\mathrm{Re}(Z_{22})$	(Ω)			4.40
R_S	(Ω)	2.17		2.08
R_D	(Ω)	2.37		2.32
R_G	(Ω)	1.70(1)	1.69(1)	1.65
n_S		1.57	1.56	1.53
n_D		1.56	1.55	
$(I_S)_S$	(pA)	3.87		
$(I_S)_D$	(pA)	3.65		

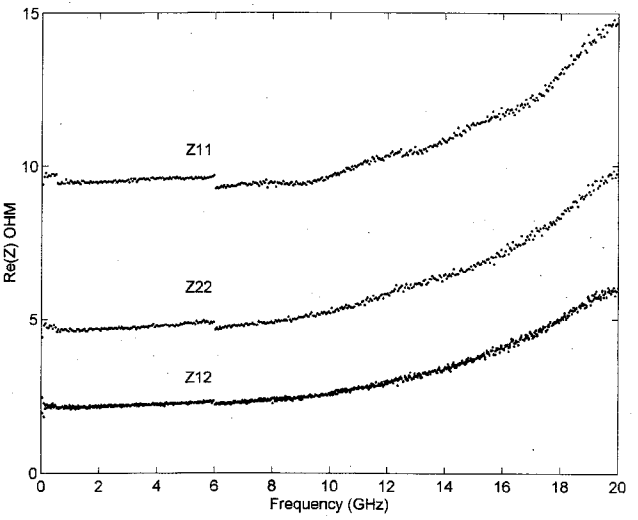

Fig. 7. Real parts of Z parameters versus frequency for microstrip-mounted transistor with floating drain at $V_{GS} > V_{bi} > 0$.

Microwave® TF 3001 K. Prior to measurements, a TRL calibration was carried out on the network analyzer using a calibration kit Intercontinental Microwave® TRL 3003.

S parameter measurements in the frequency range 0.045–20 GHz were performed on the same PHEMT as above, at the bias condition $V_{GS} > V_{bi} > 0$ with floating drain (open drain condition), for different gate currents 6 mA $< I_{GS} <$ 7 mA. These values of I_{GS} are not as high as to degrade the transistor [10] and [13].

Z parameters were calculated after transformation of the measured S parameters. The variations of $\mathrm{Re}(Z_{ij})$ against

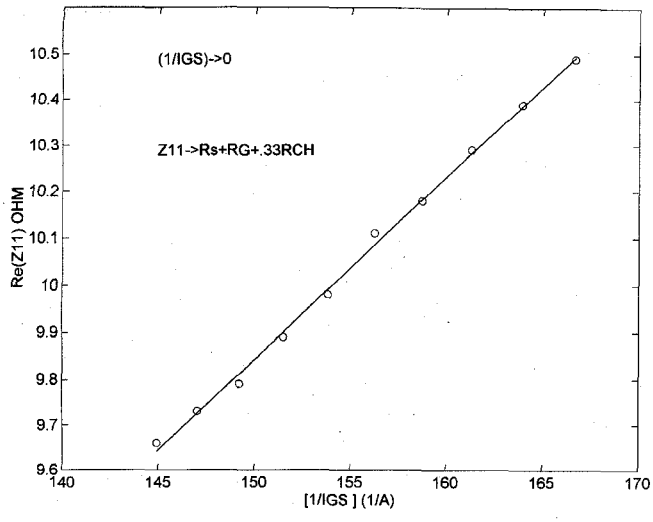

Fig. 8. Real part of Z_{11} parameter versus $1/I_{GS}$ for microstrip-mounted transistor with floating drain at $V_{GS} > V_{bi} > 0$.

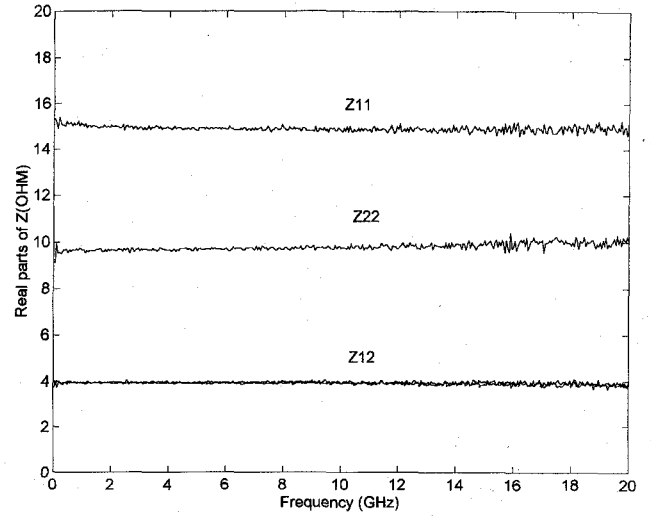

Fig. 9. Real parts of Z parameters versus frequency for on-wafer transistor with floating drain at $V_{GS} > V_{bi} > 0$.

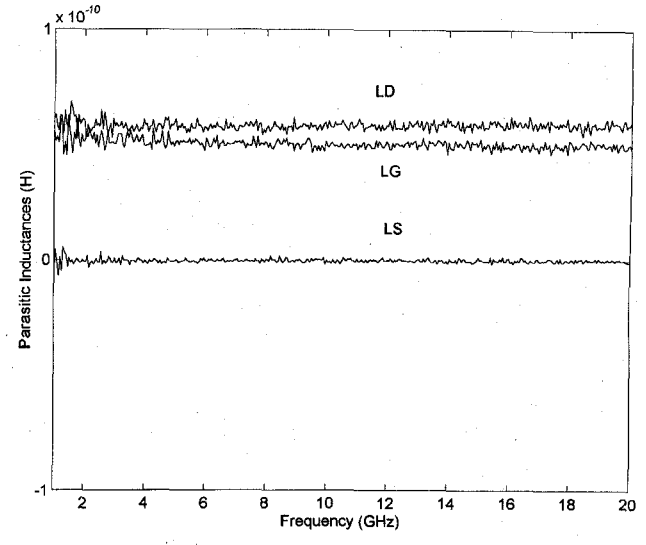

Fig. 10. Frequency dispersion of parasitic inductances for on-wafer transistor.

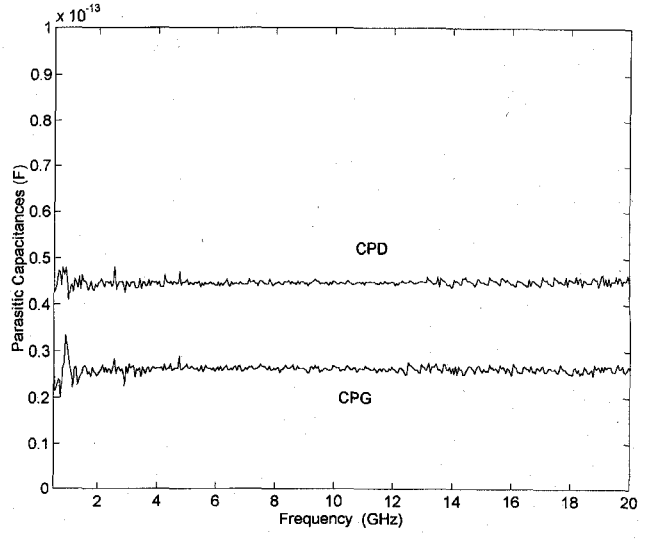

Fig. 11. Frequency dispersion of parasitic capacitances for on-wafer transistor.

frequency with floating drain are plotted in Fig. 7. It is noticed that at low frequencies, in the frequency range 0.045–10 GHz, $\mathrm{Re}\,(Z_{ij})$ are constant, as predicted by the theory. Then, parasitic resistances were computed from $\mathrm{Re}\,(Z_{ij})$ values in this frequency range. On the other hand, the plot of $\mathrm{Re}\,(Z_{11})$ versus $1/I_{GS}$ at open drain is shown in Fig. 8. As expected by the theory, the curve obtained is a straight line.

Access resistances are reported in Table I along with $\mathrm{Re}(Z_{ij})$ values used for their computation as well as the Schottky diode ideality factor. It is noted that R_S, R_D, and n_S values computed from RF and DC methods agree within 2–4%.

C. RF Method Performance in the Extraction of the Small-Signal Equivalent Circuit

As an example of the RF method performance, all small-signal equivalent circuit elements are extracted for a medium power on-wafer $\mathrm{n^+GaAs/In_{0.25}Ga_{0.75}As/n^+Al_{0.28}Ga_{0.72}As}$ PHEMT ($W_g = 120\,\mu$m, $L_g = 0.33\,\mu$m) supplied by Hewlett-Packard. In this case, a LRM calibration was carried out on the network analyzer using Picoprobes® (model 50A-GSG-150-P) as well as ISS standards from Cascade Microtech®.

Z parameters, computed from S parameter measurements at open drain under forward gate current ranging between $8\,\mathrm{mA} < I_{GS} < 9\,\mathrm{mA}$, are used for the calculation of access resistances and parasitic inductances. According to the procedure outlined in this paper, R_S, R_D, and R_G are estimated from $\mathrm{Re}\,(Z_{ij})$. Their values are equal to: $R_S = 3.9\,\Omega$, $R_D = 5.6\,\Omega$, and $R_G = 0.51\,\Omega$. Fig. 9 shows the plot of $\mathrm{Re}\,(Z_{ij})$ versus frequency. It is noticed that, for this on-wafer PHEMT, $\mathrm{Re}\,(Z_{ij})$ remains constant in the whole frequency range up to 20 GHz.

Fig. 10 reports the plot against frequency of parasitic inductances L_S, L_D, and L_G, calculated from $\mathrm{Im}\,(Z_{ij})$ using (52)–(57). As indicated in these equations, prior to the computation of parasitic inductances, parasitic capacitances must be determined.

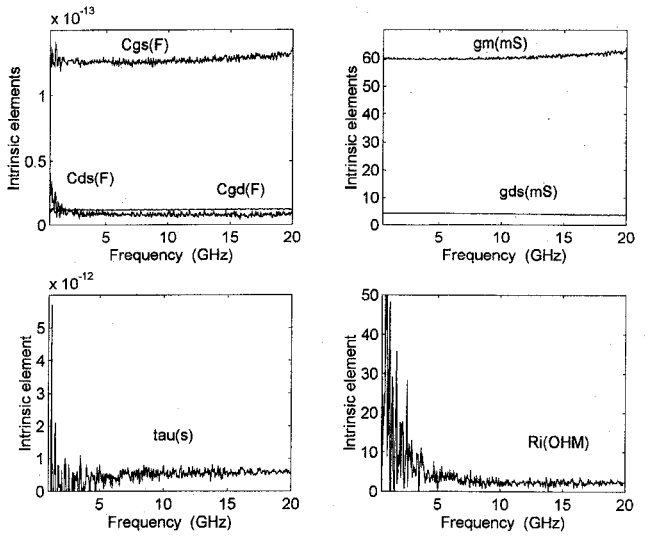

Fig. 12. Frequency dispersion of intrinsic elements for on-wafer transistor.

According to the method put forward by [2], Y parameters, calculated from S parameter measurements at $V_{DS} = 0$ and $V_{GS} = 4V_P$ (V_P = pinch-off voltage), are used for the estimation of parasitic capacitances. Fig. 11 shows the curves of C_{PD} and C_{PG} versus frequency.

On the other hand, after de-embedding all parasitic elements from S parameter measurements at $V_{DS} = 2$ V and $V_{GS} = 0$ V, intrinsic elements are extracted at this bias condition according to the Berroth and Bosh method [3] and using the circuit topology in Fig. 1(a). This topology was adopted because it yielded the best S parameter fitting. This result does not agree with those of literature [5], [6] since circuit topologies in Fig. 1(b) and (c) have been advised for coplanar transistors. Further investigation is needed to clarify the discrepancies about circuit topology. All intrinsic elements at $V_{DS} = 2$ V and $V_{GS} = 0$ V are plotted against frequency in Fig. 12. In addition, from Figs. 9–12, except for R_i and τ, no frequency dispersion is observed for extrinsic nor intrinsic elements. This behavior indicates that the circuit topology in Fig. 1(a) is suitable for the transistor under test.

As for R_i and τ, their values exhibit a large scattering at low frequencies. Owing to the small value of C_{GS} at low frequencies, large uncertainty errors are expected in the extraction of R_i from $\mathrm{Re}\,(Y_{11})$. Besides, since the value of R_i is needed for τ parameter estimation, large uncertainty errors are also expected at low frequencies. So, from Fig. 12, measurements at frequencies larger than 10 GHz are suitable for R_i and τ computation. At low frequencies, the calculation of these parameters may be improved by either, increasing up to 120 points the measurement points average in the network analyzer, or using the method proposed by [16].

VI. Conclusion

Access resistances and parasitic inductances are crucial elements in the de-embedding procedure carried out for the intrinsic elements extraction. In this paper, three methods for the computation of access resistances are investigated. Two of them are based on DC measurements with floating drain or source while the last one is based on RF measurements with floating drain. The originality of the proposed DC methods lies on the gate resistance calculation after a Schottky diode model. On the other hand, thanks to the floating drain configuration instead of the $V_{DS} = 0$ condition, the inconsistencies between DC and RF techniques are overcome. Given that the RF estimation of access resistances is reliable, an alternative method is presented for extracting the small-signal equivalent circuit on PHEMT's. This method is based on RF measurements only and uses no optimization procedures. Besides, regarding parasitic inductances, this method involves improved equations at open drain configuration that are an extension to those of Dambrine *et al.* [2].

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References

[1] F. Lin and G. Kompa, "FET model parameter extraction based on optimization with multiplane data-fitting and bidirectional search—A new concept," *IEEE Trans. Microwave Theory Tech.*, vol. 42, no. 7, pp. 1114–1121, July 1994.

[2] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, no. 7, pp. 1151–1159, July 1988.

[3] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 38, no. 7, pp. 891–895, July 1990.

[4] R. L. Vaitkus, "Uncertainty in the values of GaAs MESFET equivalent circuit elements extracted from measured two-port scattering parameters," in *Proc. 1983 IEEE Cornell Conf. High-Speed Semiconductor Dev. and Circ.*, 1983, pp. 301–308.

[5] P. Jansen, D. Schreurs, W. De Raedt, B. Nauwelaers, and M. Van Rossum, "Consistent small-signal and large-signal extraction techniques for heterojunction FET's," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 1, pp. 87–93, Jan. 1995.

[6] P. C. Walters, R. D. Pollard, J. R. Richardson, and G. Gatti, "Millimeter-wave device modeling differences in microstrip and coplanar waveguide," in *1993 IEEE MTT-S Int. Microwave Symp. Dig.*, June 1993, vol. 3, pp. 1173–1176.

[7] H. Fukui, "Determination of the basic device parameters of a GaAs MESFET," *Bell System Tech. J.*, vol. 58, no. 3, pp. 771–797, Mar. 1979.

[8] K. W. Lee, K. Lee, M. S. Shur, T. T. Vu, P. C. T. Roberts, and M. J. Helix, "Source, drain, and gate series resistances and electron saturation velocity in ion-implanted GaAs FET's," *IEEE Trans. Electron Devices*, vol. ED-32, no. 5, pp. 987–992, May 1985.

[9] S. Chaudhuri and M. B. Das, "An investigation of the MESFET 'end' resistance using a distributed diode/resistance model," *IEEE Trans. Electron Devices*, vol. ED-32, no. 11, pp. 2262–2268, Nov. 1985.

[10] R. Vogel, "The application of RF wafer probing to MESFET modeling," *Microwave J.*, vol. 31, no. 11, pp. 153–162, Nov. 1988.

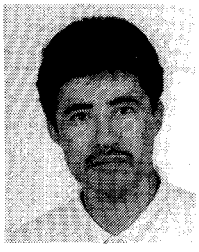
[11] J. C. Costa, M. Miller, M. Golio, and G. Norris, "Fast, accurate, on-wafer extraction of parasitic resistances and inductances in GaAs MESFET's and HEMT's," in *1992 IEEE MTT-S Int. Microwave Symp. Dig.*, June 1992, vol. 2, pp. 1011–1014.

[12] R. Tayrani, J. E. Gerber, T. Daniel, R. S. Pengelly, and U. L. Rodhe, "A new and reliable direct parasitic extraction method for MESFET's and HEMT's," in *23rd Euro. Microwave Conf.*, pp. 451–453, 1993.

[13] B.-S. Kim and S. Nam, "An iterative parasitic extraction method for HEMT," in *25th Euro. Microwave Conf.*, pp. 558–561, 1995.

[14] R. J. Bennett, "Interpretation of forward bias behavior of Schottky barriers," *IEEE Trans. Electron Devices*, vol. ED-34, no. 4, pp. 935–937, Apr. 1987.

[15] S. K. Cheung and N. W. Cheung, "Extraction of Schottky diode parameters from forward current-voltage characteristics," *Appl. Phys. Lett.*, vol. 49, no. 2, pp. 85–87, July 1986.
[16] E. Arnold, M. Golio, M. Miller, and B. Beckwith, "Direct extraction of GaAs MESFET intrinsic element and parasitic inductance values," in *1990 IEEE MTT-S Int. Microwave Symp. Dig.*, May 1990, vol. 1, pp. 359–362.



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